CLAIMS

What is claimed is:

1. An apparatus, comprising:

two or more parallel carry chain structures within an integrated circuit, each of said carry chain structures comprising a series of logical structures, at least one of said logical structures within each of said carry chain structures having an associated input node, output node and carry node, said input node corresponding to a function input term, said output node corresponding to an output term of said function; said carry node corresponding to a carry term to a following logical structure in said series of logical structures.

2. The apparatus of claim 1 wherein said associated input node for one of said carry chain structures is connected to said associated input node for another of said carry chain structures.

3. The apparatus of claim 1 wherein said logical structure comprises a look up table.

4. The apparatus of claim 3 wherein said look up table is a three input look up table.

5. The apparatus of claim 1 wherein a first functional unit within a first logical structure performs the same logical operation as a second functional unit within a second logical structure, said first logical structure within a first carry

chain that is parallel to a second carry chain, said second carry chain having said second logical structure.

6. The apparatus of claim 3 wherein said logical structure comprises two look up tables.

7. The apparatus of claim 6 wherein said carry node is coupled to one of said look up tables and said output node is coupled to the other of said look up tables.

8. The apparatus of claim 1 wherein said function is an incrementer.

9. The apparatus of claim 1 wherein said function is an adder.

10. The apparatus of claim 1 wherein said logical structure comprises logic associated with a standard cell.

11. A computer readable medium having stored thereon a data structure associated with a semiconductor design tool, comprising:

two or more parallel carry chain structures, each of said carry chain structures comprising a series of logical structures, at least one of said logical structures within each of said carry chain structures having an associated input node, output node and carry node, said input node corresponding to a function input term, said output node corresponding to an output term of said function; said carry node corresponding to a carry value to a following logical structure in said series of logical structures.

12. The machine readable medium of claim 11 wherein said associated input node for one of said carry chain structures is connected to said associated input node for another of said carry chain structures.

13. The machine readable medium of claim 11 wherein said logical structure comprises a look up table associated with programmable logic technology.

14. The machine readable medium of claim 13 wherein said look up table is a three input look up table.

15. The machine readable medium of claim 13 wherein a first functional unit within a first logical structure performs the same logical operation as a second functional unit within a second logical structure, said first logical structure within a first carry chain that is parallel to a second carry chain, said second carry chain having said second logical structure.

16. The machine readable medium of claim 13 wherein said logical structure comprises two look up tables.

17. The machine readable medium of claim 16 wherein said carry node is coupled to one of said look up tables and said output node is coupled to the other of said look up tables.

18. The machine readable medium of claim 11 wherein said function is an incrementer.

19. The machine readable medium of claim 11 wherein said function is an adder.

20. The machine readable medium of claim 11 wherein said logical structure comprises logic associated with a standard cell.

21. A method, comprising:

a) presenting input terms of a function to a two or more parallel carry chain structures;

b) executing each of said two or more parallel carry chain structures in parallel;

c) collecting the output terms of said function from said two or more parallel carry chain structures.

22. The method of claim 21 wherein all of said input terms are presented to each of said two or more parallel carry chain structures.

23. The method of claim 21 wherein a carry term produced by a logical structure associated with one of said carry chain structures is ANDed, within another logical structure associated with said one of said carry chain structures, with one of said input terms.

24. The method of claim 23 wherein said AND produces another carry term.

25. The method of claim 21 wherein said function is an incrementer.

26. A method, comprising:

a) searching for a carry chain within a semiconductor device design;

b) determining a first propagation delay through a found carry chain found, said found carry chain found from said searching;

c) determining a second propagation delay through a parallel carry chain implementation of said found carry chain; and

d) replacing said found carry chain within said semiconductor device design with said parallel carry chain implementation if said second propagation delay is lower than said first propagation delay.

27. The method of claim 26 wherein said semiconductor device design is an RTL netlist.

28. The method of claim 29 wherein said pre-determined amount is 50% of said first propagation delay.

29. The method of claim 26 further comprising searching for a second carry chain within said semiconductor device design after said replacing.

30. The method of claim 26 wherein said found carry chain and said parallel carry implementation perform the function of an incrementer.

31. The method of claim 26 wherein said found carry chain and said parallel carry implementation perform a decoding function for a multiplexer within a multiplier.

32. A method comprising:

within a semiconductor device design environment, responding to a selection of a function by implementing at least a portion of said function as one or more parallel carry chains.

33. The method of claim 32 wherein said at least a portion of said function determines channel select values for a multiplexer within a multiplier.

34. A machine readable medium having stored thereon sequences of instructions which are executable by a digital processing system, and which, when executed by the digital processing system, cause the system to perform a method comprising:

a) searching for a carry chain within a semiconductor device design;

b) determining a first propagation delay through a found carry chain found, said found carry chain found from said searching;

c) determining a second propagation delay through a parallel carry chain implementation of said found carry chain; and

d) replacing said parallel carry chain implementation within said semiconductor device if said second propagation delay is lower than said first propagation delay.

35. The machine readable medium of claim 34 wherein said semiconductor device design is an RTL netlist.

36. The machine readable medium of claim 35 further comprising compiling a behavioral level netlist to produce said RTL netlist.

37. The machine readable medium of claim 34 further comprising searching for a second carry chain within said semiconductor device design after said replacing.

38. The machine readable medium of claim 34 wherein said found carry chain and said parallel carry implementation perform the function of an incrementer.

39. The machine readable medium of claim 34 wherein said found carry chain and said parallel carry implementation perform a decoding function for a mutliplexer within a multiplier.

40. A machine readable medium having stored thereon sequences of instructions which are executable by a digital processing system, and which, when executed by said digital processing system, cause said system to perform a method, comprising:

within a semiconductor device design environment, responding to a selection of a function by implementing at least a portion of said function as one or more parallel carry chains.

41. The method of claim 40 wherein said at least a portion of said function determines channel select values for a multiplexer within a multiplier.

42. An apparatus, comprising:

a multiplexer that produces partial products within a multiplier that multiplies a first word and a second word, said multiplier having a first channel select input coupled to a first carry chain output and a second channel select input coupled to a second carry chain output.

43. The apparatus of claim 42 wherein said multiplexer further comprises a selectable channel input of 0.

44. The apparatus of claim 42 wherein said multiplexer further comprises a selectable channel input that corresponds to said word being non shifted.

45. The apparatus of claim 44 wherein said first and second carry chains have input terms corresponding to coefficients of said second word.

46. The apparatus of claim 43 wherein said multiplexer further comprises a selectable channel input that corresponds to said word being shifted.

47. The apparatus of claim 46 wherein said first and second carry chains have input terms corresponding to coefficients of said second word.

48. The apparatus of claim 42 wherein said multiplexer further comprises a selectable channel input that corresponds to a logical inverse of said first word.

49. The apparatus of claim 48 wherein said first and second carry chains have input terms corresponding to coefficients of said second word.

50. A machine readable medium having stored thereon sequences of instructions which are executable by a digital processing system, and which, when executed by the digital processing system, cause the system to perform a method comprising:

a multiplexer that produces partial products within a multiplier that multiplies a first word and a second word, said multiplier having a first channel select input coupled to a first carry chain output and a second channel select input coupled to a second carry chain output.

51. The machine readable medium of claim 50 wherein said multiplexer further comprises a selectable channel input of 0.

52. The machine readable medium of claim 51 wherein said multiplexer further comprises a selectable channel input that corresponds to said word being non shifted.

53. The machine readable medium of claim 52 wherein said first and second carry chains have input terms corresponding to coefficients of said second word.

54. The machine readable medium of claim 51 wherein said multiplexer further comprises a selectable channel input that corresponds to said word being shifted.

55. The machine readable medium of claim 54 wherein said first and second carry chains have input terms corresponding to coefficients of said second word.

56. The machine readable medium of claim 42 wherein said multiplexer further comprises a selectable channel input that corresponds to a logical inverse of said first word.

57. The apparatus of claim 48 wherein said first and second carry chains have input terms corresponding to coefficients of said second word.